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VLSI Floorplanning Algorithm Based on Reinforcement Learning with Obstacles.

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SUMMARY

This paper uses Sequence Pair (SP) encoding to represent the floorplan structure and leverages RL's ability to learn autonomously and generalize to perform floorplanning. The proposed algorithm is tested on MCNC and GSRC benchmarks, and the experimental results demonstrate that it produces better floorplan solutions.

INTRODUCTION

This paper uses the SP method to represent the floorplan structure and proposes a VLSI floorplanning algorithm based on obstructed reinforcement learning. Under certain constraints where some modules have already been placed, this algorithm defines the RL algorithm's state, action, and reward function. The experimental results show that compared with traditional SA algorithms, the proposed algorithm can effectively reduce the floorplan's total area and total wire length, resulting in better floorplan results.

APPROACH

Figure 1 shows a floorplan corresponding to a sequence pair (<3,0,2,5,4,1), (<5,0,1,2,3,4>) consisting of six blocks. The size of each block is as follows: 0(4 × 3), 1(4 × 2), 2(3 × 3), 3(7 × 3), 4(3 × 7), and 5(6 × 3). It can be seen from the figure that all blocks satisfy the above constraint relationship.

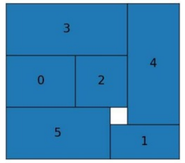

Fig. 1. A floorplan representation by SP.

METHODS

Reinforcement learning is the learning of a mapping from states to actions to maximize numerical reward. Essentially all reinforcement learning satisfies the Markov Decision Process (MDP), MDP relies on the Markov assumption, which states that the future state distribution depends only on the current state. A typical Markov decision process is shown in Figure 2.

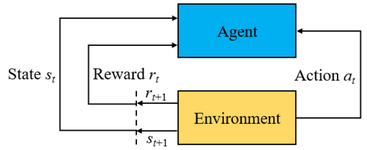

Fig. 2. A typical framework of an MDP.

RESULTS

Table 1. Comparison of experimental results of MCNC test circuit.

MCNC	Area ($\times 10^6$)		Wirelength ($\times 10^5$)		DS (%)	
	Ours	SA	Ours	SA	Ours	SA
apte	47.82	48.73	0.52	0.61	2.63	4.45
xerox	20.75	21.59	0.57	0.68	6.75	10.38
hp	9.26	9.52	0.41	0.55	4.66	7.25
ami33	1.27	1.32	0.68	0.81	8.66	12.12
ami49	38.95	41.52	6.47	6.79	8.99	14.62
Average	23.46	24.51	1.73	1.89	6.34	9.76
Normalization	1.000	1.045	1.000	1.092	1.000	1.034

Table 2. Comparison of experimental results of GSRC test circuit.

GSRC	Area ($\times 10^5$)		Wirelength ($\times 10^5$)		DS (%)	
	Ours	SA	Ours	SA	Ours	SA
n100	1.98	2.23	1.97	2.21	9.09	19.28
n200	2.15	2.37	3.46	3.87	18.14	25.74
n300	3.42	3.78	5.03	5.66	20.18	27.78
Average	2.52	2.79	3.49	3.91	15.80	24.27
Normalization	1.000	1.107	1.000	1.112	1.000	1.085

ANALYSIS

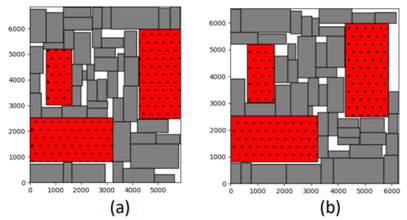

Fig. 2. Comparison of ami49 circuit floorplan results.

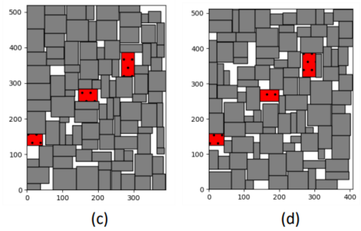

Fig. 3. Comparison of n100 circuit floorplan results.

DISCUSSION

Table 1 and Table 2 present a comparison of the experimental results for the MCNC and three GSRC test circuits. The proposed algorithm has certain advantages over the SA algorithm in optimizing floorplan area and wire length for the MCNC and GSRC benchmark circuits.

The floorplan of the ami49 test circuit generated by our algorithm (a) and SA algorithm (b) is shown in Figure 2. The floorplan of the n100 test circuit generated by our algorithm (c) and SA algorithm (d) is shown in Figure 3. From these two figures, it is evident that the area of our algorithm's floorplan is smaller than the area of the SA algorithm's floorplan.

CONCLUSIONS

This paper researches the floorplanning problem in the integrated circuit design process and proposes a VLSI floorplanning algorithm based on reinforcement learning with obstacles. Through experiments with a test circuit set, the results show that the proposed algorithm is superior to the traditional SA algorithm, and can effectively reduce the total chip area and wire length.

ACKNOWLEDGMENTS

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